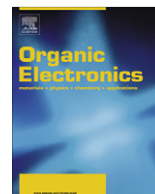




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Influences of textures in Pt counter electrode on characteristics of dye-sensitized solar cells

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ARTICLE INFO

Article history:

Received 2 September 2011
Received in revised form 7 October 2011
Accepted 23 October 2011
Available online 19 November 2011

Keywords:

DSSCs
Counter electrode
Texture
Platinum

ABSTRACT

We report an effective and yet simple way to produce nanotextures in Pt counter electrodes of dye-sensitized solar cells (DSSCs) by simply depositing Pt thin films on convenient textured substrates, and investigate the influences of textures in Pt counter electrodes on characteristics and performances of DSSCs. Pt counter electrodes having varied textures were characterized for their morphological and electrochemical properties, and were subjected to device studies to establish the correlation between Pt textures and DSSC characteristics/performances. The results suggest that the highly textured Pt electrodes can effectively enhance active surface areas and the catalytic ability for I_3^- ions reduction and charge exchange at the Pt/electrolyte interface of a DSSC. As a result, the quantum efficiency, short-circuit current, and power conversion efficiency of the DSSC were enhanced by 9–10% with using the highly textured, large-roughness, and high-surface-area Pt counter electrodes.

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1. Introduction

Since Grätzel and his colleagues reported the dye-sensitized solar cell (DSSC) [1], it had attracted much attention due to its various merits, such as the relatively high efficiencies, simple device structures, facile fabrication, potential low cost, and variety and flexibility in applications [2–5]. These features have made DSSCs attractive for solar energy applications in facing the increasing energy and environmental challenges [6–8].

A typical DSSC consists of a transparent conductive substrate, a porous thin-film photoelectrode composed of TiO_2 nanoparticles, dyes, an electrolyte, and a counter electrode [9]. The counter electrode, as one important component in DSSCs, is usually composed of a conductive catalytic layer. The role of the conductive catalytic layer as the counter electrode of the DSSC is to catalyze the reduction of the

I_3^- ions in the electrolyte produced during the regeneration of the oxidized dyes (through the oxidation of iodide ions in the electrolyte). The requirements for the counter electrode in a DSSC are thus low charge-transfer resistance and high exchange current densities for reduction of the oxidized species, and good chemical/electrochemical stability in the electrolyte systems used in DSSCs [10]. Among various materials used for counter electrodes of DSSCs [11–19], Pt is most effective due to its excellent electrocatalytic activity for reduction of triiodide. Researchers had thus been engaged in investigating different depositions of Pt counter electrodes and their influences on DSSC characteristics. For instance, researchers had studied effects of different Pt thicknesses and effects of various deposition techniques, such as physical vapor-phase deposition, electrodeposition, electrochemical deposition and thermal decomposition etc. [20–23]. On the other hand, although producing textures in the Pt counter electrode to increase its surface area also appears an effective way to enhance the catalytic capability of the counter electrode and thus

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the DSSC efficiency, yet not much systematic studies had been conducted.

In this work, we report a simple and effective way to produce nanotextures in the Pt counter electrode by depositing Pt thin films on substrates with nanotextured surfaces. The Pt counter electrodes having varied textures were characterized for their physical and electrochemical properties and were subjected to device studies. Results show that highly textured Pt counter electrodes provide larger reactive surface areas between the Pt and the electrolyte and are beneficial to conversion efficiencies of DSSCs.

2. Experiments

2.1. Preparation and characterization of textured Pt counter electrodes

Three substrates having different textures were used to deposit Pt counter electrodes and thus to prepare Pt counter electrodes having different textures, as schematically illustrated in Fig. 1. Substrate #1 was a flat glass substrate, while substrates #2 and #3 having different surface textures were glass substrates coated with the textured transparent conductor fluorine-doped tin oxide (FTO). The textured FTO substrate #2 (Solaronix, TCO 22-15, with a sheet resistance of $15 \Omega/\square$) and #3 (Solaronix, TCO 30-8, with a sheet resistance of $8 \Omega/\square$) were purchased from commercial sources. Their properties obtained from characterizations described below are summarized in Table 1. On these different substrates, Pt (15 nm thick) were deposited by e-beam evaporation to produce Pt counter electrodes having different textures (Fig. 1).

Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) were used to characterize the morphology, surface topography and roughness of the different pristine substrates. After the deposition of Pt thin films on different substrates, SEM and AFM were conducted again to

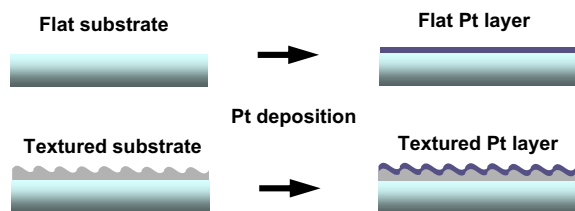


Fig. 1. Schematic illustration of the fabrication of textured Pt counter electrodes.

characterize the morphology, surface topography and roughness of the Pt counter electrodes. The sheet resistances of various counter electrodes were measured by the Van der Pauw method.

Electrochemical activities of the counter electrode for I_3^- reduction were examined by cyclic voltammetry (CV). The cyclic voltammetry was employed to characterize the relative catalytic ability/active surface areas of the Pt counter electrodes having different textures. The CV measurements were conducted using a three-electrode electrochemistry system (Gamry Instrument) and a scan rate of 100 mV/s. The electrolyte was the acetonitrile solution containing 10 mM LiI, 1 mM I_2 , and 100 mM $LiClO_4$. The Pt counter electrodes under testing were used as the working electrode, Pt foil as the counter electrode, and Ag/Ag^+ as the reference electrode [15].

2.2. DSSC fabrication

Fig. 2 shows the schematic device structure of the DSSCs using Pt counter electrodes having different textures. In fabrication of devices, the FTO glass substrates (Solaronix, TCO 22-15, with a sheet resistance of $15 \Omega/\square$) were first cleaned in a detergent solution using an ultrasonic bath and then were rinsed with water and ethanol. A layer of 20-nm-sized anatase TiO_2 nanoparticles was then coated on the FTO by the doctor-blade method. After drying the film at 120 °C, another layer of 400-nm-sized anatase TiO_2 nanoparticles was then coated as the light scattering layer. The resulting working electrode was composed of a 12- μ m-thick transparent TiO_2 nanoparticle layer (average particle size: 20 nm) and a 4- μ m-thick TiO_2 scattering layer (average particle size: 400 nm) [24]. The thickness of the TiO_2 nanoparticle layer had been optimized by balancing the tradeoff between optical absorption and the electrical transport properties. The nanoporous TiO_2 electrodes were then heated in an atmospheric oven first by gradually ramping the temperature from 150 to 500 °C and then at 500 °C for 30 min. After cooling, the nanoporous TiO_2 electrodes were immersed into a dye solution at room temperature for 24 h for dye adsorption. The dye solution was composed of 0.5 mM ruthenium dye N719, [cis-di(thiocyanato)-N-N'-bis(2,2'-bipyridyl-4-carboxylic acid-4'-tetrabutyl-ammonium carboxylate) ruthenium (II)] [25], and 0.5 mM chenodeoxycholic acid (CDCA, as a co-adsorbent) in the acetonitrile/*tert*-butanol mixture (1:1) [26].

Counter-electrodes of the DSSC were prepared by depositing 15-nm-thick Pt films on the different textured substrates by e-beam evaporation as described in the previous section. The dye-adsorbed TiO_2 working electrode and the

Table 1

Characteristics of different substrates and Pt electrodes, and DSSCs fabricated on these different Pt counter electrodes.

Characteristics of substrates and Pt electrodes						Characteristics of DSSCs				
Substrate	Substrate roughness (nm)	Pt film roughness (nm)	Pt film surface area (cm^2)	CV I_{pc} (mA/cm^2)	Pt sheet resistance (ohm/sq)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF	Eff. (%)	R_{pt} (ohm)
#1	0.18	0.21	0.126	1.78	10	15.78	0.74	0.67	7.78	9.72
#2	9.14	9.64	0.134	2.06	12	16.13	0.74	0.68	8.18	5.96
#3	28.34	28.31	0.146	2.78	8	16.64	0.74	0.69	8.49	4.55

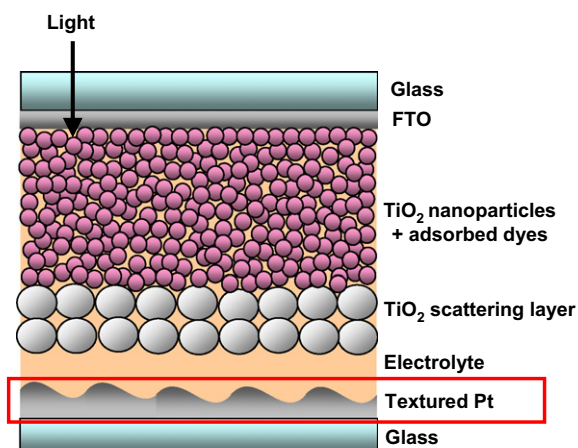


Fig. 2. The schematic device structure of the DSSC using the textured Pt as the counter electrode.

counter electrode were then assembled into a sealed DSSC cell with a sealant spacer between the two electrode plates. A drop of electrolyte solution [0.6 M 1-butyl-3-methylimidazolium iodide (BMII), 0.03 M I₂, 0.5 M 4-tert-butylpyridine, and 0.1 M guanidinium thiocyanate in a mixture of acetonitrile–valeronitrile (85:15, v/v)] was injected into the cell through a drilled hole. Finally, the hole was sealed using the sealant and a cover glass.

2.3. DSSC characterization

The photocurrent–voltage (I – V) characteristics of the DSSCs were measured under illumination of the simulated AM1.5G solar light from a 300-W Xenon lamp solar simulator. The incident light intensity was calibrated to 100 mW/cm² by using a reference Si photodiode equipped with an IR-cutoff filter (KG-5, Schott) to reduce the spectrum mismatch in the region of 350–750 nm between the simulated light and AM 1.5G to less than 2%. The reference cell is certificated by Bunkoh-keiki Co. Ltd., Japan. Photocurrent–voltage curves were obtained by applying an external bias voltage to the cell and measuring the generated photocurrent. The current–voltage characteristics of DSSCs were used to extract the short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF), and power conversion efficiency (Eff.) of the DSSCs [27,28]. The incident photon-to-current conversion efficiency (IPCE) spectra of the devices were measured by using a 75-W Xenon arc lamp as the light source coupled to a monochromator. The IPCE data were taken by illuminating monochromatic light on the solar cells (with the wavelength from 300 to 800 nm) and measuring the short-circuit current of the solar cells [29]. The IPCE measurement was performed with a lock-in amplifier, a low speed chopper, and a bias light source under the full computer control.

In addition to the standard I – V and IPCE characterizations of solar cells, in this study, the electrochemical impedance spectroscopy (EIS) was also used to analyze the internal impedance properties of DSSCs [30,31]. The electrochemical impedance spectroscopy of the cells was

measured by using an impedance analyzer with a frequency range of 20 Hz to 1 MHz. In this study, during the impedance measurement, the cell was under the constant AM 1.5G 100 mW/cm² illumination. The impedance of the cell (throughout the frequency range of 20 Hz to 1 MHz) was then measured by applying a bias at the open-circuit voltage V_{oc} of the cell (namely, under the condition of no dc electric current) and by using an ac amplitude of 10 mV.

3. Results and discussions

3.1. Properties of textured Pt counter electrodes

Fig. 3 shows the SEM and AFM images of the surfaces of substrates #1–3, respectively. In SEM images, one sees that substrate #1 (flat glass) has a flat surface, substrate #2 shows grain sizes of about 100–200 nm, and substrate #3 is composed of a mixture of larger grains and smaller grains. In substrate #3, the sizes for smaller grains and larger grains are ~100–200 and ~300–400 nm, respectively. Furthermore, larger grains in substrate #3 exhibit the distinct pyramidal shape. Topographical characteristics examined by AFM for #1–3 substrates are similar to/consistent with those observed by SEM. Yet the surface roughness can now be quantitatively determined from the AFM results. Substrate #1 shows the smallest surface roughness of 0.18 nm, substrate #2 shows a surface roughness of 9.14 nm, and substrate #3 containing larger grains shows a significantly greater surface roughness of 28.34 nm. The surface roughnesses of these substrates are summarized in Table 1.

Fig. 4 shows the SEM and AFM images of surfaces of the Pt films (15 nm thick) deposited on substrates #1–3. As can be seen from both SEM and AFM images, after coating the thin Pt films, all samples retained surface morphologies and topographies similar to those of pristine substrates #1–3. The results clearly indicate that one can effectively produce textured Pt counter electrodes by simply depositing Pt thin films on convenient textured substrates (like the textured FTO glass substrates that can easily accessed), providing an effective and yet simple way to prepare textured counter electrodes for efficient DSSCs. From AFM results, the Pt electrode on substrate #1 shows the smallest surface roughness of 0.21 nm, the Pt electrode on substrate #2 shows a surface roughness of 9.64 nm, and the Pt electrode on substrate #3 shows a significantly greater surface roughness of 28.31 nm. The surface roughnesses of the Pt electrodes are summarized in Table 1, in which one also sees that the thin Pt electrodes retained surface roughnesses similar to those of the pristine substrates. Furthermore, the surface areas of the textured Pt electrodes can be quantitatively determined from the AFM results. In Fig. 4b, the scanned area (projected area) for each Pt electrode is 4 μ m² (i.e., 2 \times 2 μ m). The calculated surface areas of Pt electrodes #1–3 are 4.03, 4.28, and 4.68 μ m², respectively. In consideration of the actual device area of 0.125 cm², the effective surface areas of the Pt electrodes #1–3 in devices are estimated to be 0.126, 0.134, and 0.146 cm², respectively. The total surface areas for the Pt electrodes used in devices are summarized in Table 1.

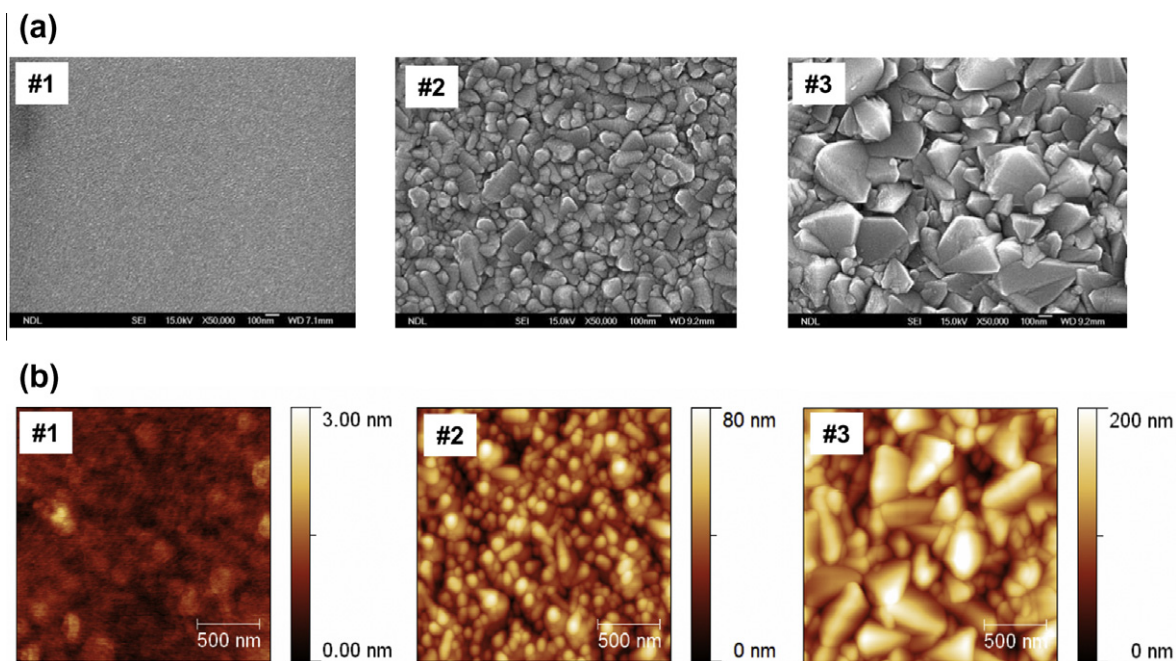


Fig. 3. (a) SEM and (b) AFM images of substrates #1–3.

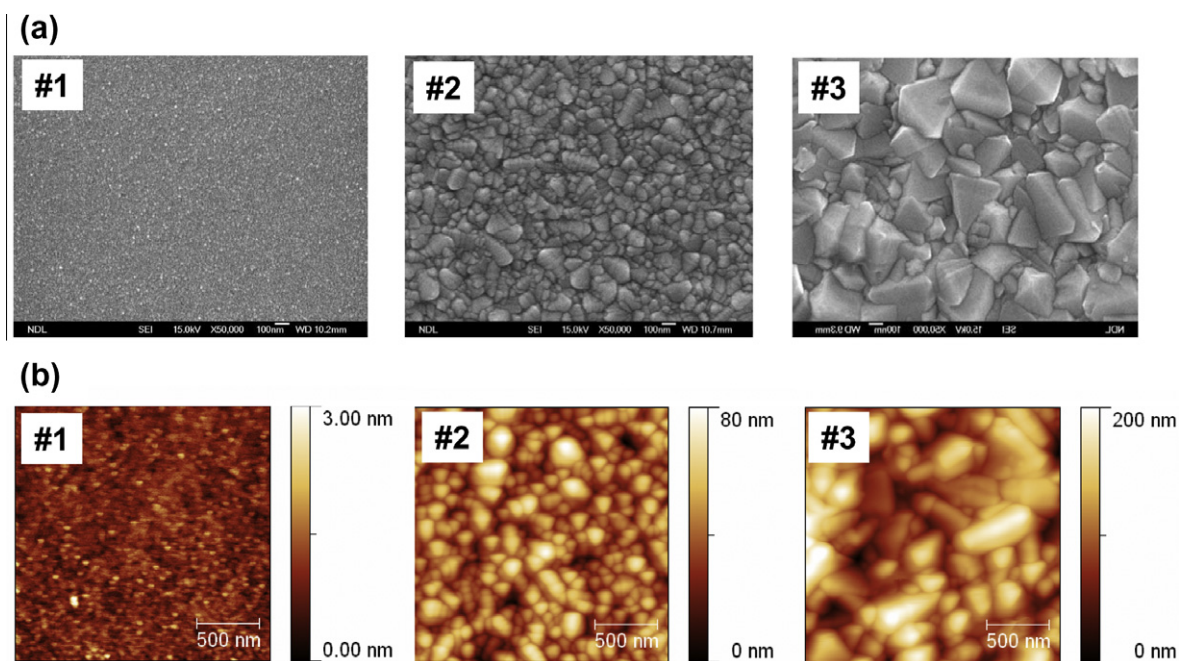


Fig. 4. (a) SEM and (b) AFM images of Pt counter electrodes deposited on substrates #1–3.

Fig. 5 shows the cyclic voltammograms from CV measurements for the Pt counter electrodes deposited on substrates having different textures. In these cyclic voltammograms, the cathodic current peaks (I_{PC}) between -0.4 and -0.6 V correspond to the reduction of I_3^- ions through interaction with the Pt electrode. Thus, in general, the magnitude of the I_{PC} represents the catalytic capability

(activity) of a counter electrode toward reduction of I_3^- in DSSCs. As seen in Fig. 5 and Table 1, the cathodic current peaks (I_{PC}) of the Pt electrodes #1–3 are 1.78, 2.06, and 2.78 mA/cm², respectively, increasing with the surface texture, surface roughness and the surface area of the Pt counter electrode. The enhanced electro-catalytic activities of #2 and #3 Pt electrodes (vs. flat Pt electrode #1) are

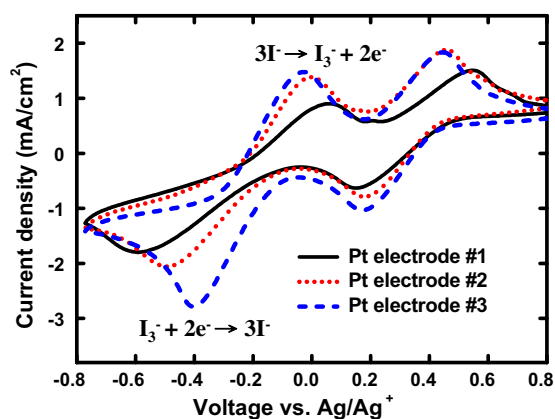


Fig. 5. Cyclic voltammograms of Pt counter electrodes deposited on substrates #1–3.

certainly associated with the increased active surface areas through deposition on textured surfaces [32]. These CV results clearly indicate that depositing Pt on textured surfaces be an effective way to increase the active surface areas of the counter electrodes and thus to enhance their electro-catalytic ability (activity).

3.2. Device characteristics of DSSCs using textured Pt counter electrodes

Fig. 6a and b shows the I – V characteristics and IPCE characteristics, respectively, of the DSSCs fabricated on the Pt counter electrodes #1–3. The photovoltaic characteristics of the three devices, including the short-circuit current (J_{SC}), the open-circuit voltage (V_{OC}), the fill factor (FF), and the conversion efficiency (Eff.), are summarized in Table 1. From Fig. 6a and Table 1, one sees that V_{OC} does not differ among these three devices. Yet, J_{SC} , FF, and power conversion efficiency of the three devices in general increases with the surface textures, the surface roughnesses and the surface areas of the Pt counter electrodes. The J_{SC} , V_{OC} and FF of the DSSC based on Pt electrode #1 are 15.78 mA cm^{-2} , 0.74 V and 0.67 , respectively, yielding an overall conversion efficiency of 7.78% . Under the same conditions, the DSSCs based on Pt electrodes #2 and #3 with larger surface textures, roughnesses, and total surface areas show enhanced J_{SC} and conversion efficiency of (16.13 mA/cm^2 , 8.18%) and (16.64 mA/cm^2 , 8.49%), respectively. The enhancements of the conversion efficiencies for DSSCs using textured Pt counter-electrodes #2 and #3 (vs. #1) are 5.14% and 9.12% , respectively.

The IPCE results of the DSSCs fabricated on the Pt counter electrodes #1–3 are shown in Fig. 6b, in which one sees that the IPCE increases with the textures of the Pt counter electrodes. The peak IPCE increases from $\sim 75\%$ of the device on Pt electrode #1, to $\sim 83\%$ of the device on Pt electrode #3. As a result, the short-circuit current J_{SC} (Fig. 6a, Table 1) also shows a corresponding enhancement in devices. Overall, the IPCE, short-circuit current, fill factor, and power conversion efficiency of the DSSCs were enhanced by using the highly textured, large-roughness, and high-surface-area Pt counter electrodes.

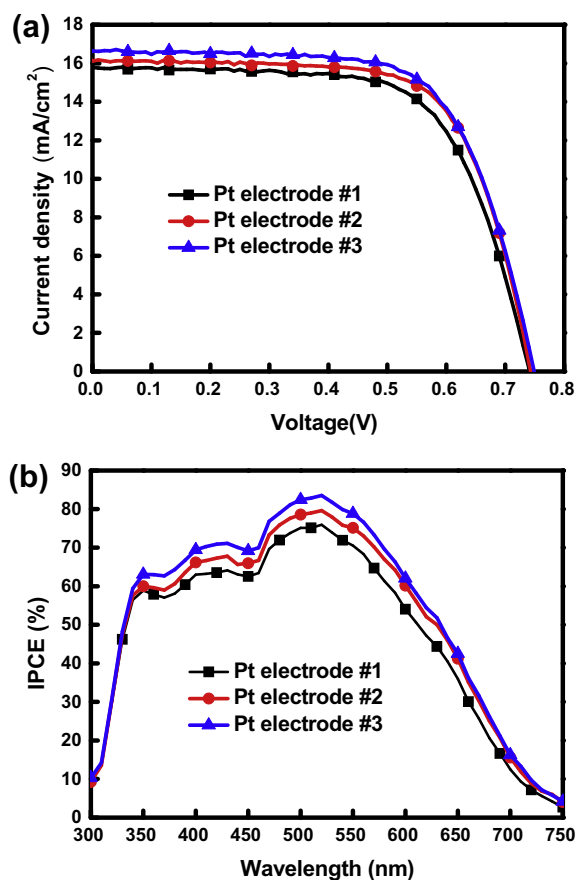


Fig. 6. (a) I – V , and (b) IPCE characteristics of DSSCs fabricated on the Pt counter electrodes #1–3.

In addition to the enhanced catalytic capability of textured Pt electrodes, other factors that might influence efficiencies, such as the difference in sheet resistance of counter electrodes or the optical scattering induced by textured Pt electrodes, were also examined. The sheet resistances of Pt counter electrodes #1–3 were measured to be 10 , 12 , and $8 \Omega/\square$, respectively (Table 1). In general, a large variation in sheet resistances (or series resistances) of counter electrodes might affect efficiencies of DSSCs. Yet, in the three cases here, the difference in sheet resistances (between 8 and $12 \Omega/\square$) is too small to influence DSSC efficiency, and indeed the device using the Pt electrode #2 (with the largest sheet resistance) still shows higher efficiency than the device using the Pt electrode #1 (with a larger sheet resistance). The textured Pt electrode could induce optical scattering and influence the DSSC efficiency, if the incident illumination could reach the counter electrode. Yet in this work, the working electrode contained a thick TiO_2 scattering layer ($4 \mu\text{m}$ thick, average particle size of 400 nm) as an optical back scattering/reflection layer, and thus the incident illumination could hardly transmit through such a TiO_2 scattering layer to reach the counter electrode (as confirmed by transmittance measurements). Thus, the optical properties of the Pt counter electrodes are not relevant in this work.

3.3. Electrochemical impedance spectroscopy of devices

The effects of textured Pt counter electrodes on photo-voltaic characteristics of DSSCs were further investigated by electrochemical impedance spectroscopy (EIS). EIS is a useful tool for characterizing interfacial charge-transfer processes in DSSCs, such as the charge recombination at the $\text{TiO}_2/\text{dye}/\text{electrolyte}$ interface, electron transport in the TiO_2 electrode, electron transfer at the counter electrode, and ion transport in the electrolyte etc. [33]. In this study, EIS was conducted by subjecting the cell to the constant AM 1.5G $100 \text{ mW}/\text{cm}^2$ illumination and to the bias at the open-circuit voltage V_{OC} of the cell (namely, the condition of no DC current).

Fig. 7 shows the EIS Nyquist plots (i.e., minus imaginary part of the impedance $-Z''$ vs. the real part of the impedance Z' when sweeping the frequency) for DSSCs using various Pt counter electrodes. In the frequency range investigated (20 Hz–1 MHz), a larger semicircle occurs in the lower frequency range ($\sim 20 \text{ Hz}$ – 1 kHz) and a smaller semicircle occurs in the higher frequency range. The larger semicircles in the lower frequency range ($\sim 20 \text{ Hz}$ – 1 kHz) are not complete due to the limited frequency range of our instrument (the lowest frequency is not low enough). With the bias illumination and voltage applied, the larger semicircle at lower frequencies corresponds to the charge transfer processes at the $\text{TiO}_2/\text{dye}/\text{electrolyte}$ interface [34], while the smaller semicircle at higher frequencies corresponds to the charge transfer processes at the Pt/electrolyte interface [35]. The smaller semicircles corresponding to the Pt electrode show significant difference between devices. It indicates that the impedance at the Pt/electrolyte interface was affected by textures in Pt counter electrodes.

By fitting the measured impedance characteristics of Fig. 7 with equivalent circuits of DSSCs [36], the charge-transfer resistances R_{Pt} (for the Pt/electrolyte interface) for DSSCs fabricated using Pt electrodes #1–3 can be extracted and are summarized in Table 1. The extracted R_{Pt} decreases from 9.72Ω of the device on Pt electrode #1 (smallest texture, roughness, and surface area) to 4.55Ω

of the device on Pt electrode #3 substrate (largest texture, roughness, and surface area). The decrease of R_{Pt} with the increase of the DSSC efficiency indicates the ability to catalyze the reduction of the I_3^- ions and thus more efficient charge exchange at the Pt/electrolyte interface are enhanced with larger Pt textures [37]. Among these Pt counter electrodes, Pt electrode #3 gives the smallest R_{Pt} , which corresponds to the highest reduction rate of the I_3^- ions due to the largest textures and highest surface areas. The EIS results are in good agreement with results of the total surface areas of Pt electrodes, the short-circuit currents, and the overall power conversion efficiencies of the DSSCs.

4. Conclusions

In conclusion, we report an effective and yet simple way to produce nanotextures in Pt counter electrodes of DSSCs by simply depositing Pt thin films on convenient textured substrates and investigate the influences of textures in platinum (Pt) counter electrodes on characteristics and performances of dye-sensitized solar cells (DSSCs). Pt counter electrodes having varied textures were characterized for their morphological and electrochemical properties and were subjected to device studies to establish the correlation between Pt textures and DSSC characteristics/performances. The results suggest that the highly textured Pt electrodes can effectively enhance active surface areas and the catalytic ability for I_3^- ions reduction and charge exchange at the Pt/electrolyte interface of a DSSC. As a result, the quantum efficiency, short-circuit current, and power conversion efficiency of the DSSC were enhanced by 9–10% with using the highly textured, large-roughness, and high-surface-area Pt counter electrodes.

Acknowledgment

The authors gratefully acknowledge the financial support from National Science Council of Taiwan.

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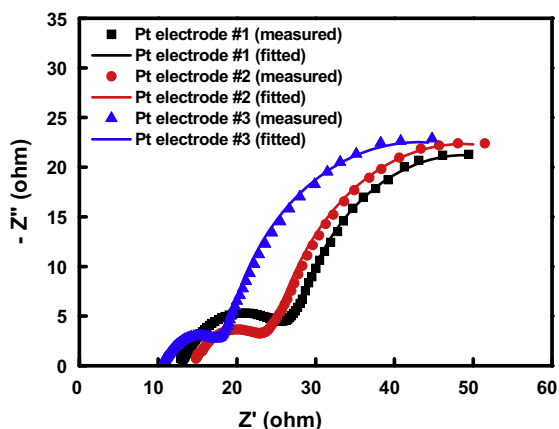


Fig. 7. Measured (symbols) and fitted (lines) EIS Nyquist plots for DSSCs fabricated on the Pt counter electrodes #1–3.

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